PATENT SPECIFICATION // DETERMINISTIC HARDWARE ACCELERATOR

Single Cache-Line Aligned Hardware Accelerator

Patent TR 2026/013786 | Granted & Active | WIPO PCT

IPC Classification: G06F 12/0862 // G06N 3/063 // H03M 7/30
Filing Date : 2026-01-28 (EPATS Priority Certified)
Architecture : Deterministic 64-Byte Zero-Stall ASIC Micro-Architecture
WCET Guarantee : <1.18 microseconds across all tensor operations

HARDWARE MICRO-ARCHITECTURE INNOVATION

Modern high-performance avionics processors suffer non-deterministic pipeline stalls caused by L1/L2 cache misses, DRAM page boundary conflicts, and bus contention. TR 2026/013786 enforces strict 64-byte single cache-line alignment directly in silicon, ensuring every tensor operand resides entirely in a single memory transaction. Result: 100.00% Zero-Stall L1 hit rate with mathematical WCET determinism.

SILICON BUS ALIGNMENT THEOREM

Stride(T) == 0 (mod 64 Bytes)

Latency_WCET < 1.18 us forall Op in Omega_Tensor

Architectural guarantees:

- Zero L1 cache line crossings: every spatial tensor block fits in 64 bytes.
- Dual-issue systolic execution array achieves zero memory-induced pipeline bubbles.
- Eliminates non-deterministic arbitration delays across shared PCIe/AXI buses.
- Guarantees predictable cycle count required by DO-254 DAL-A certification.

ISO/IEC 17025 VERIFIED SILICON BENCHMARKS

Metric Description	Standard Avionics DSP	5DVRAI TR 2026/013786	Performance Gain
Hardware Execution Cycles	34,200 cycles	2,183 cycles	15.67x Faster
Worst-Case Latency (WCET)	42.60 us	1.12 us (<1.18 us limit)	38.0x Determinism
L1 Cache Hit Ratio	82.40%	100.00% (Zero Stall)	+17.60% Zero Waste
Numerical Precision (RMSE)	0.0890	0.0019	46.8x Accuracy
Bus Contention Probability	17.6%	0.00% (Isolated Stride)	Completely Eliminated

SYNTHESIS TARGETS & HARDWARE SUPPORT:

- Fully synthesized in SystemVerilog / VHDL for Xilinx UltraScale+, AMD Versal, and TSMC 7nm.
- Drop-in AXI4-Stream slave interface compatible with RAD750 and PowerPC mission computers.